IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Gerald L. Dybsetter et al.	)
Serial No.:	10/814,392	)
Filed:	March 31, 2004	)
Confirmation No.:	5366	) Art Unit) 2185
For:	CONTINGENT PROCESSOR TIME DIVISION MULTIPLE ACCESS OF MEMORY IN A MULTI-PROCESSOR SYSTEM TO ALLOW SUPPLEMENTAL MEMORY CONSUMER ACCESS	)
Examiner:	Yaima Campos	)
Appeal No.:	_____	)

The Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

BRIEF OF APPELLANT

This is an appeal to the Board of Patent Appeals and Interferences (the "Board") from the Final Office Action mailed January 10, 2007 (the "Final Office Action") wherein the Examiner rejected claims 1-42. This Brief is being filed pursuant to the provisions of 37 C.F.R. § 41.37. This Brief is accompanied by the requisite fee of $500.00, as provided by 37 C.F.R. § 41.20(b)(2). The Commissioner is hereby authorized to charge any additional fees associated with this communication, or to credit any overpayment, to Deposit Account No. 23-3178.

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LIST OF REFERENCES

U.S. PATENT DOCUMENTS

U.S. Patent No. 6,401,176 to *Fadavi-Ardekani, et al.*
U.S. Patent No. 5,893,153 to *Tzeng, et al.*
U.S. Patent No. 6,275,885 to *Chin, et al.*

I. REAL PARTY IN INTEREST

The real party in interest comprises FINISAR CORPORATION, by way of assignment from Gerald L. Dybsetter and Jayne C. Hahin. The corresponding assignment document was recorded in the United States Patent and Trademark Office at Reel/Frame 015669/0208 on August 9, 2004. The named inventors, Gerald L. Dybsetter and Jayne C. Hahin, who are captioned in the present application, assigned their interest in the present application to FINISAR CORPORATION.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 1-42 were rejected in the Final Office Action mailed January 10, 2007 (the "Final Office Action"). Indicated status of claims is as of the mailing date of the Final Office Action. Claims 1-42 are being appealed.

IV. STATUS OF AMENDMENTS

The Appellant has not submitted any amendments subsequent to the Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

It should be noted that nothing in the following discussion is intended, nor should be used, to construe the scope or meaning of any of the claims. Rather, the following discussion, and corresponding references to the specification and figures, are provided solely for informational purposes so as to comply with the formal requirements of 37 CFR § 41.37(c)(1)(v).

In the example of claim 1, a method is claimed for a memory controller (102) to manage access for a plurality of processors (110) and one or more other memory consumers (120) to a system memory (101). *See, e.g.*, pages 8-11, paragraphs [0021]-[0028]; *see also* Figures 1-3. The plurality of processors (110) and the one or more other memory consumers (120) each accesses the system memory (101) through the memory controller (102). The method includes an act (301) of the memory controller (102) allotting a first division (221) of each of a plurality of memory access cycles (200) to time-division multiple access of the system memory (101) for a first processor (111) of the plurality of processors (110) such that memory access is guaranteed for the first processor (111) during the first division (221) of each of the plurality of memory access cycles (200). *See, e.g.*, pages 10 and 11, paragraph [0027]; *see also* Figure 3, act 301. The method also includes an act (302) of the memory controller (102) allotting a second division (222) of each of the plurality of memory access cycles (200) to time-division multiple access of the system memory (101) for a second processor (112) of the plurality of processors (110) such that memory access is conditionally granted to the second processor (112) during the second division (222) of each of the plurality of memory access cycles (200) subject to a determination that at least one of the one or more other memory consumers (120) has not also requested access to the system memory (101). *See, e.g.*, page 11, paragraph [0028]; *see also* Figure 3, act 302.

In the example of claim 20, a system includes a system memory (101), a memory controller (102) that governs access to the system memory (101), a plurality of processors (110) that each accesses the system memory (101) through the memory controller (102), and one or more other memory consumers (120) that also each accesses the system memory (101) through the memory controller (102). *See, e.g.*, pages 8 and 9, paragraphs [0021] and [0022]; *see also* Figure 1. The memory controller (102) is configured to perform an act (301) of allotting a first division (221) of each of a plurality of memory access cycles (200) to time-division multiple access of the system memory (101) for a first processor (111) of the plurality of processors (110) such that memory access is guaranteed for the first processor (111) during the first division (221) of each of the plurality of memory access cycles (200). *See, e.g.*, pages 10 and 11, paragraph [0027]; *see also* Figure 3, act 301. The memory controller (102) is also configured to perform an act of allotting a second division (222) of each of the plurality of memory access cycles (200) to time-division multiple access of the system memory (101) for a second processor (112) of the plurality of processors (110) such that memory access is conditionally granted to the second processor (112) during the second division (222) of each of the plurality of memory access cycles (200) subject to a determination that at least one of the one or more other memory consumers (120) has not also requested access to the system memory (101). *See, e.g.*, page 11, paragraph [0028]; *see also* Figure 3, act 302.

In the example of claim 28, a memory controller (102) is configured to perform various acts when operated in a system that includes a system memory (101) for which the memory controller (102) governs access, and a plurality of processors (110) and one or more other memory consumers (120) that each accesses the system memory (101) through the memory controller (102). *See, e.g.*, pages 8 and 9, paragraphs [0021] and [0022]; *see also* Figure 1. The

memory controller (102) is configured to perform an act of allotting a first division (221) of each of a plurality of memory access cycles (200) to time-division multiple access of the system memory (101) for a first processor (111) of the plurality of processors (110) such that memory access is guaranteed for the first processor (111) during the first division (221) of each of the plurality of memory access cycles (200). *See, e.g.*, pages 10 and 11, paragraph [0027]; *see also* Figure 3, act 301. The memory controller (102) is also configured to perform an act of allotting a second division (222) of each of the plurality of memory access cycles (200) to time-division multiple access of the system memory (101) for a second processor (112) of the plurality of processors (110) such that memory access is conditionally granted to the second processor (112) during the second division (222) of each of the plurality of memory access cycles (200) subject to a determination that at least one of the one or more other memory consumers (120) has not also requested access to the system memory (101). *See, e.g.*, page 11, paragraph [0028]; *see also* Figure 3, act 302.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Issue 1: Whether claims 1-6 and 9-33 are unpatentable, under 35 U.S.C. §103(a), as being obvious over U.S. Patent No. 6,401,176 to Fadavi-Ardekani, et al. ("*Fadavi-Ardekani*") in view of U.S. Patent No. 5,893,153 to Tzeng, et al. ("*Tzeng*").

Issue 2: Whether claims 7 and 8 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* and *Tzeng* as applied to claim 6, and further in view of U.S. Patent No. 6,275,885 to Chin, et al. ("Chin").

Issue 3: Whether claims 34 and 40-42 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* and *Tzeng* as applied to claim 28, and further in view of assertions by the Examiner that it would have been obvious to use the memory controller as claimed in these claims.

Issue 4: Whether claims 35-39 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* and *Tzeng* as applied to claim 28, and further in view of assertions by the Examiner that it would have been obvious to apply the memory controller as claimed in these claims to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater than 10 G.

VII. ARGUMENT

A. Issue 1: Whether claims 1-6 and 9-33 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* in view of *Tzeng*.

It is well settled that in order to establish a *prima facie* case of obviousness, it is the burden of the Examiner to demonstrate that three criteria are met: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; second, there must be a reasonable expectation of success; and third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *M.P.E.P. § 2143*. For at least the reasons set forth below however, the Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 1-6 and 9-33.

i. The Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 1-6 and 9-33

a. Claims 1, 20, and 28

As noted in both Applicants' paper filed on October 30, 2006 ("*Applicants' October 30, 2006 Paper*") and Applicants' Pre-Appeal Brief Request for Review ("*Applicants' Pre-Appeal Brief Request*"), the Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 1, 20, and 28. *Applicants' October 30, 2006 Paper* at 13-15; *Applicants' Pre-Appeal Brief Request*, at 2-4.

For example, each of the rejected independent claims 1, 20, and 28 require that a "memory controller" perform or be configured to perform:

> an act of [] allotting a first division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a first processor of the plurality of processors such that memory access is guaranteed for

the first processor during the first division of each of the plurality of memory access cycles; and

an act of [] allotting a second division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor during the second division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

(Emphasis added). Thus, each of the rejected independent claims 1, 20, and 28 require that "each of a plurality of memory access cycles" be divided into at least "a first division" and "a second division" with memory access during the first division being "guaranteed" for a first processor and memory access during the second division being "conditionally granted" to a second processor.

In general, Applicants understand that the Examiner has characterized one of the various "super agents" in the systems of *Fadavi-Ardekani* as corresponding to the "first processor" and the various "non-super agents" in *Fadavi-Ardekani* as corresponding to the "second processor" and the "other memory consumers" recited in claims 1, 20, and 28. *See, e.g., Final Office Action*, at 6 ("Fadavi-Ardekani discloses these limitations as memory access to a super agent (*first processor, as claimed by Applicant*) is given without having to arbitrate with non-super agents (*second processor or other memory [consumer] devices as claimed by applicant*)...") (emphasis in original). It is apparent that the systems of *Fadavi-Ardekani* allow only one agent to access memory at any given time. *See* column 3, lines 53-55 ("An arbiter and switch 102 allows *one* of the plurality of agents 100 or 104 to access the shared synchronous memory 200 *at any one time*.").

In light of the foregoing, it thus appears to be the position of the Examiner that one of the super agents of *Fadavi-Ardekani* is allotted "a first division of each of a plurality of memory

access cycles...such that memory access is guaranteed for the first processor during the first division" and that one of the non-super agents of *Fadavi-Ardekani* is allotted "a second division of each of the plurality of memory access cycles...such that memory access is conditionally granted for the second processor during the second division..." as required by claims 1, 20, and 28.

Despite the assertions of the Examiner, however, *Fadavi-Ardekani* does not teach that a non-super agent is allotted "a second division of each of the plurality of memory access cycles...such that memory access is conditionally granted to" the non-super agent "during the second division." Instead, *Fadavi-Ardekani* teaches that a super agent can access memory "*whenever requested*," which necessarily includes "during the second division of each of [a] plurality of memory access cycles." For example, *Fadavi-Ardekani* teaches "The predetermined rules provide that the super agent A is provided transparent access to the shared synchronous memory 200, i.e., *whenever desired*." Column 5, lines 62-65 (emphasis added). *Fadavi-Ardekani* also teaches:

> The arbiter and switch 102 monitors accesses by the super agent A to the shared synchronous memory 200, e.g., to determine open windows wherein the super agent A would not be affected by an access to the shared synchronous memory 200 by another agent. The non-super agent B can submit memory request signals to the arbiter and switch 102 at any time. However, for this non-super agent B, ownership of the shared synchronous memory is granted on a cycle-by-cycle basis of the clock signal *only when access by the super agent A is not necessary*.

Column 5, lines 50-59 (emphasis added). *Fadavi-Ardekani* also teaches:

> Thus, in accordance with the principles of the present invention, one of a plurality of agents accessing a shared synchronous memory is given a super agent priority. The super agent can access the shared synchronous memory without negotiation and/or arbitration. However, the remaining non-super agents can access the memory only when it is available, i.e., when the shared synchronous memory *is not being used by the super agent*.

> The use of a super agent non-super agent distinction between a plurality of agents accessing a shared synchronous memory improves upon the degraded performance otherwise experienced by the overall system and in particular the super agent because of the overhead inherent in an arbitration process. With higher priority, the super agent is given access to the shared synchronous memory *whenever requested* and can thus access the shared synchronous memory *without halting its operation*."

Column 8, lines 41-57 (emphasis added). *Fadavi-Ardekani* also teaches that, "The present invention has particular application in shared memory systems wherein it is preferred that a main agent access a shared synchronous memory *without interruption or disruption*." Column 12, lines 32-35.

Therefore, despite the Examiner's assertions to the contrary, *Fadavi-Ardekani* does not teach that "each of a plurality of memory access cycles" be divided into at least "a first division" and "a second division" with memory access during the first division of a memory access cycle being "guaranteed" to a first processor and memory access during the second division of the same memory access cycle being "conditionally granted" to a second processor, as required by claims 1, 20, and 28.

Instead, *Fadavi-Ardekani* teaches various priority-based systems where super agents are assigned a higher priority than non-super agents, and memory access is granted on a higher-priority-first basis. Instead of "allotting a second division of each of a plurality of memory access cycles" for one or more non-super agents (i.e. a second processor or other memory consumer, according to the Examiner), the systems of *Fadavi-Ardekani* allow access by a super agent (i.e. a first processor, according to the Examiner) "*whenever requested*." *See, e.g.*, column 8, lines 54-57 ("...the super agent is given access to the shared synchronous memory *whenever requested* and can thus access the shared synchronous memory *without halting its operation*.").

Thus, *Fadavi-Ardekani* *teaches away* from having an allotted "second division of each of a plurality of memory access cycles" for non-super agents (i.e. a second processor or other memory consumer, according to the Examiner) because such an allotted portion of each memory access cycle for non-super agents would prevent the super agent (i.e. a first processor, according to the Examiner) from gaining memory access "*whenever requested*" or "*whenever desired*," resulting in "*interruption or disruption*" of the super agent and "*halting [of] its operation*." Therefore, the Examiner's characterization of *Fadavi-Ardekani* as teaching the above-recited limitations is logically inconsistent. It is noted that combining *Fadavi-Ardekani* and *Tzeng* in the purportedly obvious fashion advanced by the Examiner does not remedy this systematic deficiency of *Fadavi-Ardekani*.

For at least the foregoing reasons, Applicants respectfully submit that the Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claim 1, 20, and 28.

b. Claims 2-5

The Examiner has also failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 2-5. For example, each of the rejected dependent claims 2-5 require that "the first division in a given memory access cycle" is "before," "after," "adjacent in time with," or "separated in time with" "the second division in the memory access cycle." By virtue of their dependence from claim 1, claims 2-5 each require that "the second division of each of the plurality of memory access cycles" be allotted "for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor..."

However, as discussed at VII.A.i.a above in connection with claim 1, and despite the Examiner's assertions to the contrary, *Fadavi-Ardekani* and *Tzeng* combined in the purportedly obvious fashion advanced by the Examiner do not teach dividing each of a plurality of memory access cycles into at least first and second divisions, with the "second division of each of the plurality of memory access cycles" being allotted for a second processor (i.e. a non-super agent, according to the Examiner) "such that memory access is conditionally granted to the second processor during the second division...," at least because *Fadavi-Ardekani* teaches that a super agent can access memory "*whenever requested*," which necessarily includes "during the second division of each of [a] plurality of memory access cycles."

Therefore, since the combination of *Fadavi-Ardekani* and *Tzeng* does not teach dividing each of a plurality of memory access cycles into at least first and second divisions as required by claim 1, the combination of *Fadavi-Ardekani* and *Tzeng* does not teach that "the first division in a given memory access cycle" is "before," "after," "adjacent in time with," or "separated in time with" "the second division in the memory access cycle" as required by claims 2-5.

For at least the foregoing reasons, Applicants respectfully submit that the Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claim 2-5.

c. Claims 16, 17, 24, and 32

The Examiner has further failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 16, 17, 24, and 32. For example, each of the rejected dependent claims 16, 17, 24, and 32 requires that a memory controller perform or be configured to perform:

> an act of [] allotting a fourth division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a fourth

> processor of the plurality of processors such that memory access is conditionally granted to the fourth processor during the fourth division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

(Emphasis added).

However, as discussed at VII.A.i.a above in connection with claims 1, 20, and 28, and despite the Examiner's assertions to the contrary, *Fadavi-Ardekani* and *Tzeng* combined in the purportedly obvious fashion advanced by the Examiner do not teach this limitation because *Fadavi-Ardekani* does not teach that "each of a plurality of memory access cycles" be divided into at least "a first division," "a second division," and "a fourth division" with memory access during the first division being "guaranteed" to a first processor and memory access during the second and fourth divisions being "conditionally granted" to a second processor and a fourth processor, respectively, as required by claims 16, 17, 24, and 32.

Instead, as discussed above, *Fadavi-Ardekani* teaches various priority-based systems where super agents are assigned a higher priority than non-super agents, and memory access is granted on a higher-priority-first basis. Instead of "allotting a fourth division of each of a plurality of memory access cycles" for one or more non-super agents (i.e. a fourth processor or other memory consumer, according to the Examiner), the systems of *Fadavi-Ardekani* allow access by a super agent (i.e. a first processor, according to the Examiner) "*whenever requested*."

Thus, *Fadavi-Ardekani* *teaches away* from having an allotted "fourth division of each of a plurality of memory access cycles" for non-super agents (i.e. a fourth processor or other memory consumer, according to the Examiner) because such an allotted portion of each memory access cycle for non-super agents would prevent the super agent (i.e. a first processor, according

to the Examiner) from gaining memory access "*whenever requested*" or "*whenever desired*," resulting in "*interruption or disruption*" of the super agent and "*halting [of] its operation*."

For at least the foregoing reasons, Applicants respectfully submit that the Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claim 16, 17, 24, and 32.

d. Claims 25 and 33

The Examiner has further failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 25 and 33. For example, each of the rejected dependent claims 25 and 33 requires that a memory controller perform or be configured to perform:

> an act of allotting a third division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of processors such that memory access is conditionally granted to the third processor during the third division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

(Emphasis added).

However, as discussed at VII.A.i.a above in connection with claims 1, 20, and 28, and despite the Examiner's assertions to the contrary, *Fadavi-Ardekani* and *Tzeng* combined in the purportedly obvious fashion advanced by the Examiner do not teach this limitation because *Fadavi-Ardekani* does not teach that "each of a plurality of memory access cycles" be divided into at least "a first division," "a second division," and "a third division" with memory access during the first division being "guaranteed" to a first processor and memory access during the second and third divisions being "conditionally granted" to a second processor and a third processor, respectively, as required by claims 25 and 33.

Instead, as discussed above, *Fadavi-Ardekani* teaches various priority-based systems where super agents are assigned a higher priority than non-super agents, and memory access is granted on a higher-priority-first basis. Instead of "allotting a third division of each of a plurality of memory access cycles" for one or more non-super agents (i.e. a third processor or other memory consumer, according to the Examiner), the systems of *Fadavi-Ardekani* allow access by a super agent (i.e. a first processor, according to the Examiner) "*whenever requested*."

Thus, *Fadavi-Ardekani* *teaches away* from having an allotted "third division of each of a plurality of memory access cycles" for non-super agents (i.e. a third processor or other memory consumer, according to the Examiner) because such an allotted portion of each memory access cycle for non-super agents would prevent the super agent (i.e. a first processor, according to the Examiner) from gaining memory access "*whenever requested*" or "*whenever desired*," resulting in "*interruption or disruption*" of the super agent and "*halting [of] its operation*."

For at least the foregoing reasons, Applicants respectfully submit that the Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claim 25 and 33.

e. Claims 6, 9-15, 18, 19, 21-23, 26, 27, and 29-31

As discussed at VII.A.i.a above, the Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 1, 20, and 28. By virtue of their dependence from one of claims 1, 20, and 28, claims 6, 9-15, 18, 19, 21-23, 26, 27, and 29-31 each require that a "memory controller" perform or be configured to perform:

> an act of [] allotting a second division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor during the second division of each of the plurality of memory access cycles subject to a determination that at least one of the one or

more other memory consumers has not also requested access to the system memory.

(Emphasis added).

As discussed at VII.A.i.a above in connection with claims 1, 20, and 28 however, even if the references are combined in the purportedly obvious fashion advanced by the Examiner, the Examiner has failed to establish that the resulting combination includes all the limitations of claims 1, 20, or 28, respectively.

For at least the foregoing reasons, Applicants respectfully submit that the Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claim 6, 9-15, 18, 19, 21-23, 26, 27, and 29-31, which each depend from one of claims 1, 20, or 28.

ii. The Examiner has failed to establish that there is a reasonable expectation of success in implementing the purportedly obvious combination of *Fadavi-Ardekani* and *Tzeng*

In view of the teaching of *Fadavi-Ardekani* that a super agent can access memory "*whenever requested*," which necessarily includes "during the second division of each of [a] plurality of memory access cycles," it is not apparent that there is a reasonable expectation that modification of the *Fadavi-Ardekani* systems with the teachings of *Tzeng* would prove to be successful. In fact, given the express teaching of *Fadavi-Ardekani* that a super agent can access memory "*whenever requested*," the modification proposed by the Examiner, to the extent understood by Applicants, may in fact compromise the functionality of the *Fadavi-Ardekani* systems. Thus, there would be no reason for one of ordinary skill in the art to make the purportedly obvious combination advanced by the Examiner.

iii. Conclusion

For at least the foregoing reasons, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 1-6 and 9-33. Accordingly, the rejection of claims 1-6 and 9-33 under 35 U.S.C. § 103(a) is not well taken and should be overruled by the Board.

B. Issue 2: Whether claims 7 and 8 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* and *Tzeng* as applied to claim 6, and further in view of U.S. Patent No. 6,275,885 to Chin et al. ("*Chin*").

i. The Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 7 and 8

In the interest of brevity, Applicants note that rejection of claims 7 and 8 are problematic for at least the same reasons set forth in the discussion of claims 6, 9-15, 18, 19 at VII.A.i.e above, and Applicants respectfully direct the attention of the Board to that discussion.

ii. The Examiner has failed to establish that there is a reasonable expectation of success in implementing the purportedly obvious combination of *Fadavi-Ardekani*, *Tzeng*, and *Chin*

In view of the teaching of *Fadavi-Ardekani* that a super agent can access memory "*whenever requested*," which necessarily includes "during the second division of each of [a] plurality of memory access cycles," it is not apparent that there is a reasonable expectation that modification of the *Fadavi-Ardekani* systems with the teachings of *Tzeng* and *Chin* would prove to be successful. In fact, given the express teaching of *Fadavi-Ardekani* that a super agent can access memory "*whenever requested*," the modification proposed by the Examiner, to the extent understood by Applicants, may in fact compromise the functionality of the *Fadavi-Ardekani* systems. Thus, there would be no reason for one of ordinary skill in the art to make the purportedly obvious combination advanced by the Examiner.

iii. Conclusion

For at least the foregoing reasons, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 7 and 8. Accordingly, the rejection of claims 7 and 8 under 35 U.S.C. § 103(a) is not well taken and should be overruled by the Board.

C. Issue 3: Whether claims 34 and 40-42 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* and *Tzeng* as applied to claim 28, and further in view of assertions by the Examiner that it would have been obvious to use the controller as claimed in these claims.

i. The Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 34 and 40-42

The Examiner has further failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 34 and 40-42.

For example, the rejected dependent claim 34 requires that a "memory controller *is implemented in* a laser transmitter/receiver." (Emphasis added). The rejected dependent claim 40 requires that "the laser transmitter/receiver is an XFP laser transceiver." The rejected dependent claim 41 requires that "the laser transmitter/receiver is an SFP laser transceiver." The rejected dependent claim 42 requires that "the laser transmitter/receiver is a SFF laser transceiver."

In his rejection of claim 34, the Examiner admits that "the combination of Fadavi-Ardekani and Tzeng does not disclose a memory controller is implemented in a laser transmitter/receiver wherein the laser transmitter/receiver might be an XFP laser transceiver, SFP laser transceiver or a SFF laser transceiver." *Final Office Action* at 11. However, the Examiner goes on to assert that "it would have been obvious ...to use the controller as being claimed in claim 30 in a laser transmitter/receiver wherein the laser transmitter/receiver might be a XFP laser transceiver, SFP laser transceiver or a SFF laser transceiver. A recitation directed to *the*

manner in which a claim is intended to be used does not distinguish the claim form the prior art if prior art has the capability to do so." *Final Office Action* at 11 (citation omitted, emphasis added).

Despite this assertion of the Examiner, it is clear from the plain language of claim 34 that claim 34 does not simply recite "the manner in which a claim is intended to be used." Rather, claim 34 requires that the memory controller "*is implemented in* a laser transmitter/receiver." The phrase "is implemented in" in claim 34 is not a statement of how the controller is intended to be used; instead, the phrase "is implemented in" requires that the memory controller be "implemented in" a laser transmitter/receiver.

For at least the foregoing reasons, Applicants respectfully submit that the Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claim 34 and 40-42.

ii. The Examiner has failed to establish that there is a reasonable expectation of success in implementing the purportedly obvious combination of *Fadavi-Ardekani* and *Tzeng*

In the interest of brevity, Applicants note that rejection of claims 34 and 40-42 are problematic for at least the same reasons set forth in the discussion of claims 28-33 at VII.A.ii above, and Applicants respectfully direct the attention of the Board to that discussion.

iii. Conclusion

For at least the foregoing reasons, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 34 and 40-42. Accordingly, the rejection of claims 34 and 40-42 under 35 U.S.C. § 103(a) is not well taken and should be overruled by the Board.

D. Issue 4: Whether claims 35-39 are unpatentable, under 35 U.S.C. §103(a), as being obvious over Fadavi-Ardekani and Tzeng as applied to claim 28, and further in view of assertions by the Examiner that it would have been obvious to apply the memory controller as claimed in these claims to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater than 10 G.

i. The Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 35-39

The Examiner has further failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 35-39.

For example, the rejected dependent claims 35-39 require that a "laser transmitter/receiver is "a 1G laser transceiver," "a 2G laser transceiver," "a 4G laser transceiver," "a 10G laser transceiver," or "a laser transceiver suitable for fiber channels greater than 10G," respectively.

In his rejection of claims 35-39, the Examiner admits that "the combination of Fadavi-Ardekani and Tzeng does not disclose expressly that a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater that 10 G." *Final Office Action* at 12. However, the Examiner goes on to allege that "it would have been obvious...to apply the controller of claim 30 to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater that 10 G. Applicant has not disclosed that applying the controller of claim 30 to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater that 10 G provides an advantage, is used for a particular purpose, or solves a stated problem." *Final Office Action* at 12.

It appears that in making this allegation however, the Examiner is improperly attempting to place a burden on the Applicants to establish patentability of the claims. It is well established, however, that the burden is on the Examiner to make a *prima facie* case that the claims are not patentable. Applicants note, moreover, that the lack of a description by the Applicants of how any one of these particular bit transfer rates "provides an advantage, is used for a particular

purpose, or solves a stated problem" is simply inadequate to serve as a foundation for a conclusion of obviousness. Applying the rationale advanced by the Examiner, an applicant could inoculate claims from a charge of obviousness merely by including in the application self-serving statements of the how a particular limitation "provides an advantage, is used for a particular purpose, or solves a stated problem." Such an approach however has no basis in logic or fact. Moreover, the Examiner has cited no authority in support of his proposition that failing to describe how a particular claim limitation "provides an advantage, is used for a particular purpose, or solves a stated problem" is sufficient to make a *prima facie* case that the claim is not patentable.

In his rejection of claims 35-39, the Examiner has further asserted that "One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with any memory size because the combination Fadavi-Ardekani and Tzeng provides a method/system/controller to control accesses to memory by a plurality of processors and other peripheral or I/O devices, regardless of the size of the memory and Fadavi-Ardekani explains that ["the principles of the present invention relate equally to all types of synchronous memory" (Column 3, lines 44-45)]." *Final Office Action* at 12.

It appears that in making this allegation however, the Examiner has misunderstood what one of ordinary skill in the art would understand the phrase "a XG laser transceiver" to mean. The "XG" limitation in claims 35-39 does not apply to the "memory size" of the transceiver. Instead, the "XG" limitation in claims 35-39 makes reference to the bit transfer rate of the transceiver. *See, e.g., Specification*, page 14, paragraph [039] ("As the principles of the present invention allow for more efficient access to system memory, processing efficiency and speed are improved. This will become increasingly important for faster *bit rates transfers*. Accordingly,

the principles of the present invention are suitable for 1G, 2G, 4G, 10G and higher bandwidth fiber channels.") (emphasis added). Therefore, the Examiner's citation to a portion of *Fadavi-Ardekani* dealing with "types of synchronous memory" is not relevant.

For at least the foregoing reasons, Applicants respectfully submit that the Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claim 35-39.

ii. The Examiner has failed to establish that there is a reasonable expectation of success in implementing the purportedly obvious combination of *Fadavi-Ardekani* and *Tzeng*

In the interest of brevity, Applicants note that rejection of claims 35-39 are problematic for at least the same reasons set forth in the discussion of claims 28-33 at VII.A.ii above, and Applicants respectfully direct the attention of the Board to that discussion.

iii. Conclusion

For at least the foregoing reasons, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 35-39. Accordingly, the rejection of claims 35-39 under 35 U.S.C. § 103(a) is not well taken and should be overruled by the Board.

CONCLUSIONS

Based on the foregoing, Appellant respectfully submits that the rejections of the claims are not well taken. Accordingly, Appellant respectfully requests that the Board reverse the Examiner's rejections of claims 1-42 pending in this application and thereby place this application in condition for immediate allowance.

DATED this the 13th day of December, 2007.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

1. **(Previously presented)** In a system that includes a system memory, and a plurality of processors and one or more other memory consumers that each accesses the system memory through a memory controller, a method for the memory controller to manage access to the system memory for each of the plurality of processors and the one or more other memory consumers, the method comprising the following:

an act of the memory controller allotting a first division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a first processor of the plurality of processors such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles; and

an act of the memory controller allotting a second division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor during the second division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

2. **(Original)** A method in accordance with Claim 1, wherein the first division in a given memory access cycle of the plurality of memory access cycles is before the second division in the given memory access cycle.

3. **(Original)** A method in accordance with Claim 1, wherein the first division in a given memory access cycle of the plurality of memory access cycles is after the second division in the given memory access cycle.

4. **(Original)** A method in accordance with Claim 1, wherein the first division in a given memory access cycle of the plurality of memory access cycles is adjacent in time with the second division in the given memory access cycle.

5. **(Original)** A method in accordance with Claim 1, wherein the first division in a given memory access cycle of the plurality of memory access cycles is separated in time with the second division in the given memory access cycle by one or more other divisions.

6. **(Original)** A method in accordance with Claim 1, further comprising the following:

an act of receiving a request to access the system memory from the second processor during the second division of the first memory access cycle of the plurality of memory access cycles;

an act of determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle; and

in response to the act of determining that at least one of the one or more other memory consumers has not also requested to access the system memory and the act of

receiving the request from the second processor, an act of imposing the request from the second processor on the system memory.

7. **(Original)** A method in accordance with Claim 6, wherein the act determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle comprises the following:

an act of concluding that the at least one of the one or more other memory consumers has not also requested access based on having received the request to access system memory from the second processor, wherein the request is not issued by the second processor if the at least one of the one or more memory consumers had requested access.

8. **(Original)** A method in accordance with Claim 6, wherein the act determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle comprises the following:

an act of concluding that the at least one of the one or more other memory consumers has not also requested access based on having received the request to access system memory from the second processor, wherein the request from the second processor is not received by the memory controller if the at least one of the one or more memory consumers had requested access.

9. **(Original)** A method in accordance with Claim 6, further comprising the following:

an act of determining that the at least one of the one or more other memory consumers has requested access to the system memory during the second division of a second memory access cycle of the plurality of memory access cycles; and

an act of allowing the at least one of the one or more other memory consumers to have access to the system memory during the second division of the second memory access cycle.

10. **(Original)** A method in accordance with Claim 9, wherein the first memory access cycle is before the second memory access cycle.

11. **(Original)** A method in accordance with Claim 9, wherein the first memory access cycle is after the second memory access cycle.

12. **(Original)** A method in accordance with Claim 9, wherein the second memory access cycle is adjacent in time with the first memory access cycle.

13. **(Original)** A method in accordance with Claim 9, wherein the second memory access cycle is separated in time with the first memory access cycle by one or more other memory access cycles.

14. **(Original)** A method in accordance with Claim 9, further comprising the following:

an act of receiving a request from the second processor to access the system memory during the second division of the second memory access cycle, wherein the act of allowing the at least one of the one or more other memory consumers to have access to the system memory during the second division of the second memory access cycles is performed regardless of having received the request from the second processor to access the system memory during the second division of the second memory access cycle.

15. **(Original)** A method in accordance with Claim 1, further comprising the following:

an act of the memory controller allotting a third division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of processors such that memory access is guaranteed for the third processor during the third division of each of the plurality of memory access cycles.

16. **(Original)** A method in accordance with Claim 15, further comprising the following:

an act of the memory controller allotting a fourth division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a fourth processor of the plurality of processors such that memory access is conditionally granted to the fourth processor during the fourth division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

17. **(Original)** A method in accordance with Claim 1, further comprising the following:

an act of the memory controller allotting a fourth division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a fourth processor of the plurality of processors such that memory access is conditionally granted to the fourth processor during the fourth division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

18. **(Original)** A method in accordance with Claim 1, wherein at least one of the one or more other memory consumers includes a serial interface.

19. **(Original)** A method in accordance with Claim 1, wherein the one or more memory consumers comprise a plurality of memory consumers.

20. **(Previously presented)** A system comprising the following:

a system memory,

a memory controller that governs access to the system memory;

a plurality of processors that each accesses the system memory through the memory controller; and

one or more other memory consumers that also each accesses the system memory through the memory controller, wherein

the memory controller is configured to perform the following:

an act of allotting a first division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a first processor of the plurality of processors such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles; and

an act of allotting a second division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor during the second division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

21. **(Original)** A system in accordance with Claim 20, wherein the memory controller is further configured to perform the following:

an act of receiving a request to access the system memory from the second processor during the second division of the first memory access cycle of the plurality of memory access cycles;

an act of determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle; and

in response to the act of determining that at least one of the one or more other memory consumers has not also requested to access the system memory and the act of receiving the request from the second processor, an act of imposing the request from the second processor on the system memory.

22. **(Original)** A system in accordance with Claim 21, wherein the memory controller is further configured to perform the following:

an act of determining that the at least one of the one or more other memory consumers has requested access to the system memory during the second division of a second memory access cycle of the plurality of memory access cycles; and

an act of allowing the at least one of the one or more other memory consumers to have access to the system memory during the second division of the second memory access cycle.

23. **(Original)** A system in accordance with Claim 20, wherein the memory controller is further configured to perform the following:

an act of allotting a third division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of processors such that memory access is guaranteed for the third processor during the third division of each of the plurality of memory access cycles.

24. **(Original)** A system in accordance with Claim 23, wherein the memory controller is further configured to perform the following:

an act of allotting a fourth division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a fourth processor of the plurality of processors such that memory access is conditionally granted to the fourth processor during the fourth division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

25. **(Original)** A system in accordance with Claim 20, wherein the memory controller is further configured to perform the following:

an act of allotting a third division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of processors such that memory access is conditionally granted to the third processor during the third division of each of the plurality of memory access cycles

subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

26. **(Original)** A system in accordance with Claim 20, wherein at least one of the one or more other memory consumers includes a serial interface.

27. **(Original)** A system in accordance with Claim 20, wherein the one or more memory consumers comprise a plurality of memory consumers.

28. **(Previously presented)** A memory controller configured to perform the following when operated in a system that includes a system memory for which the memory controller governs access, and a plurality of processors and one or more other memory consumers that each accesses the system memory through the memory controller:

an act of allotting a first division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a first processor of the plurality of processors such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles; and

an act of allotting a second division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor during the second division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

29. **(Original)** A memory controller in accordance with Claim 28, further configured to perform the following:

an act of receiving a request to access the system memory from the second processor during the second division of the first memory access cycle of the plurality of memory access cycles;

an act of determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle; and

in response to the act of determining that at least one of the one or more other memory consumers has not also requested to access the system memory and the act of receiving the request from the second processor, an act of imposing the request from the second processor on the system memory.

30. **(Original)** A memory controller in accordance with Claim 29, further configured to perform the following:

an act of determining that the at least one of the one or more other memory consumers has requested access to the system memory during the second division of a second memory access cycle of the plurality of memory access cycles; and

an act of allowing the at least one of the one or more other memory consumers to have access to the system memory during the second division of the second memory access cycle.

31. **(Original)** A memory controller in accordance with Claim 28, further configured to perform the following:

an act of allotting a third division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of processors such that memory access is guaranteed for the third processor during the third division of each of the plurality of memory access cycles.

32. **(Original)** A memory controller in accordance with Claim 31, further configured to perform the following:

an act of allotting a fourth division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a fourth processor of the plurality of processors such that memory access is conditionally granted to the fourth processor during the fourth division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

33. **(Original)** A memory controller in accordance with Claim 28, further configured to perform the following:

an act of allotting a third division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of processors such that memory access is conditionally granted to the third processor during the third division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory.

34. **(Original)** A memory controller in accordance with Claim 28, wherein the memory controller is implemented in a laser transmitter/receiver.

35. **(Original)** A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a 1G laser transceiver.

36. **(Original)** A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a 2G laser transceiver.

37. **(Original)** A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a 4G laser transceiver.

38. **(Original)** A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a 10G laser transceiver.

39. **(Original)** A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a laser transceiver suitable for fiber channels greater than 10G.

40. **(Original)** A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is an XFP laser transceiver.

41. **(Original)** A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is an SFP laser transceiver.

42. **(Original)** A memory controller in accordance with Claim 34, wherein the laser transmitter/receiver is a SFF laser transceiver.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None (*see* II. above).